29.2 A Linear Regulator with Fast Digital Control for Biasing Integrated DC-DC Converters

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Reduced switching losses in submicron CMOS processes have enabled the design of DC-DC converters with nanosecond response times [1] and efficiencies of 95% [2]. The gate oxide breakdown voltage limits the input voltage V_{IN} of the converter to 1.2V in a 90nm CMOS process. Figure 29.2.1 shows that V_{IN} can be doubled by connecting two bridge transistors in series to share the voltage stress [3]. This scheme requires an auxiliary regulator to supply the center rail for the drivers and bridges. We considered a 12W DC-DC converter that operates from V_{IN}=2.4V in a 1.2V process. While the average current drawn by the drivers is only 80mA, a peak current of ±16A was observed during switching. In a 16-phase configuration the peak current is reduced to ±1A. A 2.4V-tolerant linear regulator was designed that supplies 1.2V/±1A. To meet a ±10% droop target at the lowest power we used a digitally-controlled regulator topology with ultra-fast response time. The sum of the regulator bias current and the leakage current of the on-chip decoupling capacitance was minimized. With a 2.4nF capacitor the total quiescent current is 25.7mA and the current efficiency is 97.5% at 1A load. The 62mW loss degrades DC-DC converter's power efficiency by only 0.5%. A measured load response time of 288ps results in a speed-power figure of merit that is 3X better than the best previously published work known to the authors [4].

Figure 29.2.2 shows a schematic diagram. The linear regulator operates in two voltage domains. Reference inverters I_0 and I_5 are connected in series between V_{IN} and ground. Reference voltage, V_{REF}, is produced between I_0 and I_5. Circuits in the $1xV_{CC}$ domain (AMP_1, ADC_1, DAC_1) are supplied between ground and V_{OUT} and circuits in the $2xV_{CC}$ domain (AMP_2, ADC_2, DAC_2) are supplied between V_{OUT} and V_{IN}. The inverters were implemented as CMOS inverters. Inverters I_0-I_2, I_5-I_7, and the comparators in ADC_1 and ADC_2 are matched and have the same trip point. Inverters I_3 and I_4 have wider NMOS devices to lower the trip point by 48mV. Inverters I_8 and I_9 have wider PMOS devices to raise the trip point by 48mV. Skewing of the trip points is indicated by an offset added to the inputs of I_3 and I_8. Gain of AMP_1 and AMP_2 is set to 5X by the relative sizes of I_1 to I_2, I_3 to I_4, I_6 to I_7, and I_8 to I_9. The 5X-amplified offset creates a 240mV drop across the resistive networks of ADC_1 and ADC_2. When V_{OUT}=V_{REF} the resistors of ADC_1 and ADC_2 are biased below and above the comparator trip points, thereby producing 16-bit thermometer codes of all ones and all zeros, respectively. The NMOS devices of DAC_1 and PMOS devices of DAC_2 are off and the output current is zero. A feedback signal from V_{OUT} couples to AMP_1 and AMP_2 via the supply rail with a gain of 0.5X. Amplifiers AMP_1 and AMP_2 amplify the signal by 5X. The comparators in ADC_1 and ADC_2 are also biased from V_{OUT} and their trip points shift by 0.5X of V_{OUT} in the same direction as the amplified feedback signal. The net signal to the comparators is 2X the variation on V_{OUT}. The ±240mV range of ADC_1 and ADC_2 corresponds to a ±120mV droop on V_{OUT}. A dead band of ±7.5mV around the unloaded value of V_{OUT} guarantees a zero cross-over current during a load current reversal.

Matching of the inverters in the reference and the amplifier portion is critical. All inverters were derived from a single layout template cell which was arrayed in 16 rows as shown in Fig. 29.2.3. Large inverters used multiple template cells connected in parallel and interleaved with other inverters. Matching of the comparator inverters is not critical because the signal is already amplified by 5X and the mismatch will only affect linearity. The LSB comparators of ADC_1 and ADC_2 can be mismatched by up to 30mV without causing cross-over current.

The linear regulator was fabricated on a 90nm CMOS process. The input-output characteristic in Fig. 29.2.4 shows tracking between V_{OUT} and V_{IN} during power-up of the circuit. Ideally, the regulator will produce V_{OUT}=1.2V with V_{IN}=2.4V. Negative body bias on inverter I_5 reduces the reference voltage to 1.146V. This difference was ignored during the design for two reasons. First, in the DC-DC converter, the PMOS in the bridge is usually larger than the NMOS so the DC level of V_{OUT} will be higher than the unloaded level and will compensate for the lower reference. Second, I_0 and I_5 of equal size guarantee similar coupling of AC noise and symmetrical AC-tracking of V_{IN}.

Figure 29.2.5 shows the DC output characteristic. Output V_{OUT} is within 100mV of the unloaded value when the load current is swept over the full range from -1A to +1A. It also shows a dead band of 15-30mV where the output current is zero.

Figure 29.2.6 shows the transient response under instantaneous load steps from zero to ±1A at 25°C. The input voltage V_{IN} and ground both experience fluctuations that correlate with the changes in the load current and are caused by series inductance in the input path of the test setup. The regulator is stable and V_{OUT} remains within 120mV of the unloaded value. The total quiescent current was 25.7mA. Measurements of 40 dies from the same wafer yielded a standard deviation of 8.2mV for the unloaded V_{OUT}. The average value of droop was 120mV with σ=4mV. The 1-σ variation in the quiescent current was <12%. At 110°C, the droop was ±134mV and the quiescent current was 31.6mA.

Figure 29.2.7 shows the chip micrograph. A push-pull load circuit was integrated on the chip to facilitate the step response measurements. The regulator and the decoupling capacitor occupy an area of 0.03mm² and 0.71mm², respectively. Assuming a cooling limit of 100W/cm², a digital circuit consuming 12W would occupy at least 12mm². The area overhead of the linear regulator would be 0.25% and the decoupling capacitor 5.9%. This decoupling capacitor also supports V_{IN} of the DC-DC converter.

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References:
[1] P. Hazucha, et al., "A 233-MHz 80%-87% Efficient Four-Phase DC-DC Converter Utilizing Air-Core Inductors on Package," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 838-845, April, 2005.
[2] J. Kim, M. A. Horowitz, "An Efficient Digital Sliding Controller for Adaptive Power-Supply Regulation," *IEEE J. Solid-State Circuits*, vol. 37, no. 5, pp. 639-647, May, 2002.
[3] J. Xiao, et al., "A 4μA-Quiescent-Current Dual-Mode Buck Converter IC for Cellular Phone Applications," *ISSCC Dig. Tech. Papers*, pp. 280-281, Feb., 2004.
[4] S. Rajapandian, et al., "High-Tension Power Delivery – Operating 0.18μm CMOS Digital Logic at 5.4V," *ISSCC Dig. Tech. Papers*, pp. 298-299, Feb., 2005.

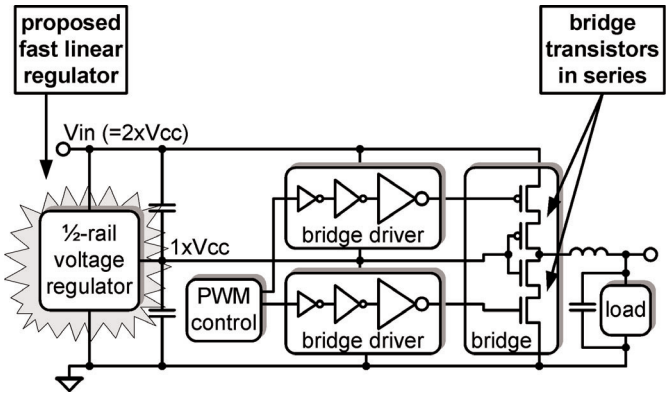

Figure 29.2.1: Linear regulator for biasing of drivers and bridges of an integrated DC-DC converter.

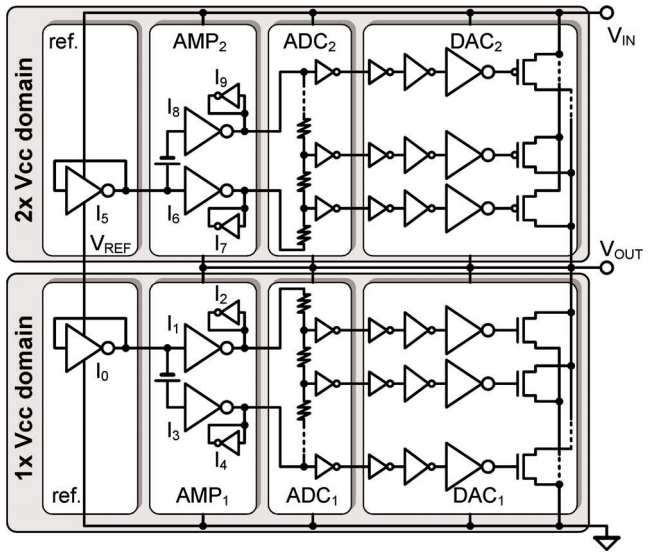

Figure 29.2.2: Schematic diagram of the linear regulator.

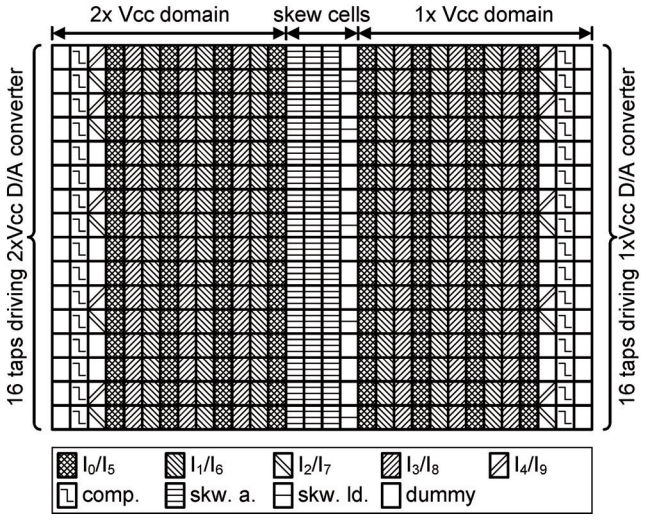

Figure 29.2.3: Floorplan of the reference and amplifiers.

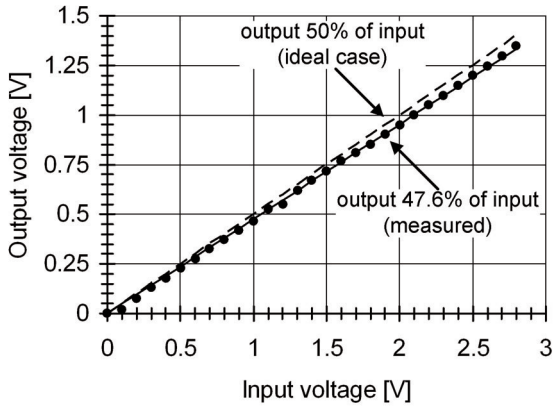

Figure 29.2.4: Measured DC input-output characteristic.

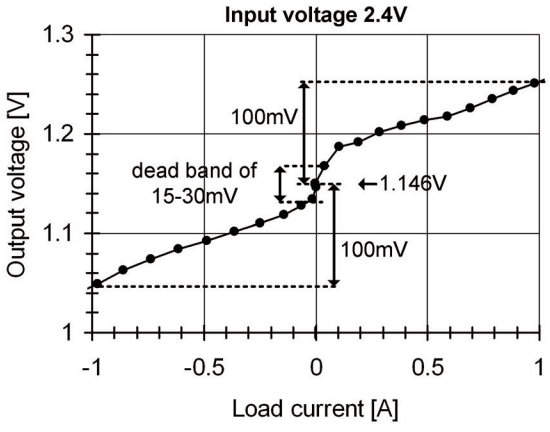

Figure 29.2.5: Measured DC output characteristic.

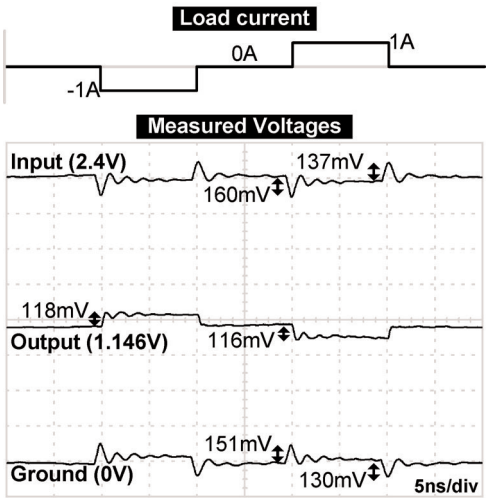

Figure 29.2.6: Measured step response at full load current.

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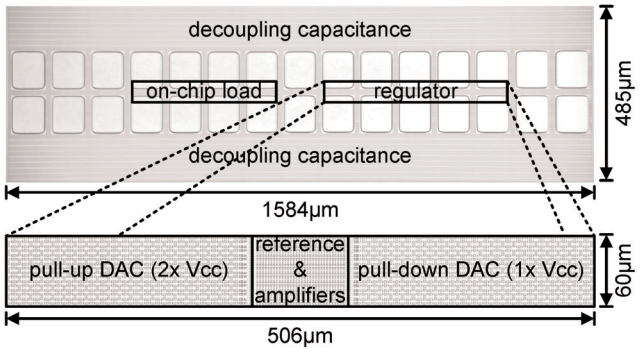

Input Voltage	2.4V	Regulator Area	0.03mm^2
Output Voltage	1.146V	Current Density	± 33A/mm^2
Maximum Load	± 1A	Output Droop	± 0.12V
Decoupling Cap.	2.4nF	Current Efficiency	97.5%
Response Time	288ps	Technology	90nm CMOS

Figure 29.2.7: Chip micrograph and summary of performance.

